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Dielectric Passivation and Edge Effects in Planar GaN Schottky Barrier Diodes

B. Orfao, B. G. Vasallo, S. Pérez, *Member, IEEE*, J. Mateos, *Member, IEEE*, D. Moro-Melgar, M. Zaknoune, and T. González, *Senior Member, IEEE*

***Abstract*— The influence of passivation on the edge effects (EEs) present in the capacitance–voltage (*C–V*) characteristics of GaN Schottky barrier diodes (SBDs) with realistic geometry is analyzed by means of Monte Carlo simulations. The enhancement of the performance of SBDs as frequency multipliers is based on the optimization of the nonlinearity of the *C–V* curve, where EEs, strongly influenced by the dielectric passivation of the diode, play a significant role and must be carefully considered. The extra capacitance associated with EEs is affected by the presence of surface charges at the semiconductor/dielectric interface, which is considered by means of a self-consistent model in which the local value of the surface charge is updated according to the surrounding electron density. Our results indicate that, in realistic SBD geometries, a higher dielectric constant of the passivation material leads to more pronounced EEs. The thickness of the dielectric and the lateral extension of the epilayer are also important parameters to be taken into account when dealing with EEs.**

***Index Terms*— Dielectric passivation, edge effects (EEs), Monte Carlo (MC), permittivity, Schottky barrier diodes (SBDs).**

I. Introduction

In THE last few years, THz technology has advanced significantly, even if difficulties for the development of massive commercial applications in the THz range are still to be solved, mainly related to signal generation. Planar Schottky barrier diodes (SBDs) fabricated on GaAs exhibit an outstanding performance as direct THz detectors and are at the base of the frequency multipliers that allow for fabricating solid-state sources and heterodyne detectors above the THz limit [1]. This allows for sensing THz radiation of extremely low power as needed, for example, in radio astronomy [2]. The wide bandgap of GaN provides this material with a high breakdown field, which, together with high electron mobility and good thermal conductivity, makes it an excellent candidate to fabricate devices, in particular, SBDs, to be used in the first stages of the multiplication chain (below 100–200 GHz) of THz frequency multipliers since they would be able to produce much higher power densities than GaAs-based devices. The most important parameter for optimizing the SBD performance acting as frequency multiplier is the nonlinearity of its capacitance–voltage (C–V) characteristic [3]. C–V curves of SBDs have been widely studied by means of 1-D Monte Carlo (MC) simulations of simple diode geometries [4], [5]. However, for high-frequency applications, the size of Schottky contacts has to be much reduced, thus being strongly affected by edge effects (EEs) that cannot be captured by a 1-D model, so that the value of its capacitance deviates from its expected ideal value [3]. Thus, in order to precisely take into account the EEs, 2-D models are needed [3], [6], [7]. Indeed, in realistic SBDs geometries, many factors may affect the contribution of EEs to the diode capacitance. In particular, in order to improve the device performance, the passivation of the GaN interfaces by means of dielectric materials is needed, thus preventing oxidation and chemical and/or electronic degradation [8], [9], and the presence of the dielectric may strongly increase the edge capacitances. On the other hand, the sharp potential drop at the edges of the Schottky contact is smoothed by the presence of the passivation dielectric so that it can be beneficial for increasing the breakdown voltage of the diodes.

The objective of this article is to report on the influence of dielectric passivation on the EEs present in realistic SBDs, including the presence of charges trapped at the passivated surfaces. To this end, MC simulations are used to obtain the distribution of the electric potential and electron concentration and calculate the edge fringing capacitance.

II. Materials and Methods

For the calculations, a semiclassical ensemble MC simulator of carrier transport self-consistently coupled with a 2-D Poisson solver has been used [10]–[12]. The conduction band of GaN is formed of three nonparabolic spherical valleys: Γ_1, U, and Γ_3 [10], [13], [14]. Ionized impurities, alloy, polar

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B. Orfao, B. G. Vasallo, S. Pérez, J. Mateos, and T. González are with the Applied Physics Department, University of Salamanca, 37008 Salamanca, Spain (e-mail: beatrizorfao@usal.es; bgvasallo@usal.es; susana@usal.es; javierm@usal.es; tomasg@usal.es).

D. Moro-Melgar is with ACST GmbH, D-63457 Hanau, Germany (e-mail: diego.moro-melgar@acst.de).

M. Zaknoune is with the Institut d'Electronique de Microélectronique et de Nanotechnologie, University of Lille, 59650 Lille, France (e-mail: mohammed.zaknoune@univ-lille.fr).

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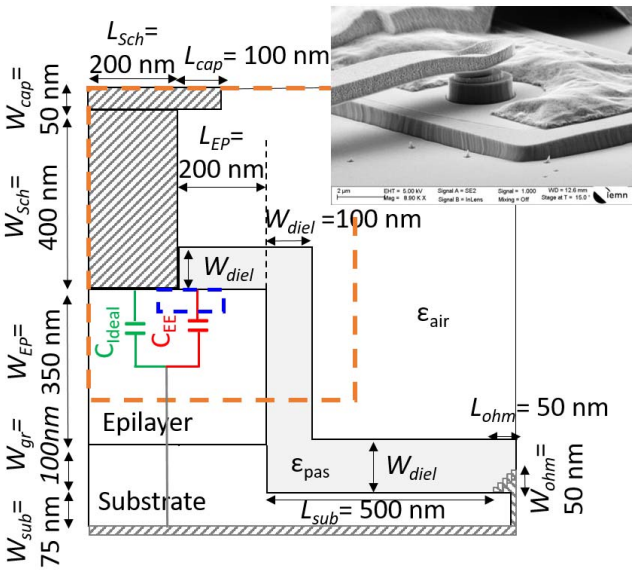

Fig. 1. Scheme of the 2-D simulated SBD including the nominal values of the different characteristic parameters of the geometry, based in real diodes, such as the one shown in the SEM image. The orange dashed rectangle is the region represented in the maps of Fig. 2, and the blue one is the area represented in Fig. 5. A simple scheme of capacitances that includes the ideal capacitance (C_{Ideal}) and the EE capacitance (C_{EE}) is represented.

and nonpolar optical phonon, acoustic phonon, and intervalley scattering mechanisms are included in the simulator. Details and parameters of the GaN model can be found in [14].

Fig. 1 shows the geometry of the simulated GaN SBD, where the nominal values of the different characteristic parameters are indicated. The simulated domain replicates the main features of a real planar diode as shown in the SEM image of the figure [15]. The layer structure consists of a highly doped substrate with doping $N_S = 5 \cdot 10^{18}$ cm^{-3} and an epilayer with doping $N_E = 3 \cdot 10^{17}$ cm^{-3}. The Schottky contact is placed on the top of the epilayer and is modeled as a perfect absorbing boundary [10], [12], [16]. The stepped ohmic contact imposes charge neutrality in the proximity of the electrode by injecting thermal carriers [17]. Simulations with different values of some geometrical parameters have been carried out in order to find the optimal configuration to reduce EEs, by focusing on parameters of the passivation material, such as the dielectric thickness (W_{diel}) or the dielectric constant (ϵ_{pas}). Air, SiO_2, silicon nitride (Si_3N_4), and a high-k dielectric (e.g., ZrO_2), with ϵ_{pas} of 1.0, 3.9, 7.5, and 25.0 [18], respectively, have been considered as passivation dielectrics in the simulations. Furthermore, a surface charge density σ is considered at the semiconductor–dielectric interfaces, modeled by means of a self-consistent charge model (SCCM) in which the local value of σ is dynamically evaluated depending on the surrounding carrier density [19]. The SCCM has been validated in previous works [19]–[22]. The total capacitance (per unit length) $C(V) = C_{\text{Ideal}} + C_{\text{EE}}$ is given by the sum of the ideal capacitance $C_{\text{Ideal}} = L_{\text{sch}} \cdot \epsilon_{\text{sc}} / W(V)$ and the EE capacitance $C_{\text{EE}} = \beta \cdot \epsilon_{\text{sc}}$ [10], [20], where ϵ_{sc} is the permittivity of the semiconductor, $W(V)$ the depth of the depletion region, and L_{sch} the length of the Schottky contact. The dimensionless parameter β, characteristic of EEs, is determined and analyzed as in [20]. β is calculated from the slope of the representation of $(Q_{\text{MC}} - Q_{\text{Id}})$ versus $(V - V_b)$, where Q_{MC} is the charge depleted by the bias voltage obtained from the MC simulations, Q_{Id} the ideal depleted charge, V the applied voltage, and V_b the built-in voltage of the Schottky contact (here considered to take a typical value of 0.8 V). By using the SCCM for the consideration of surface charges, two EE parameters can be determined depending on the charges included in the calculation of the EE capacitance: β_e, which is given just by the charge associated with the variation in the number of electrons inside the diode, and β_T, which is associated with the variation of the total charge, including as well the variation of the surface charge [20]. The trapping/release of electrons in surface deep traps associated with the variations of the surface charge included in our SCCM are slow processes and are expected to have effect only when operating at low-frequency. For that reason, β_T is the parameter to be considered in low-frequency applications (frequencies at which the surface charge follows the variation of the signals) and β_e in high-frequency applications (surface charges no longer responding to changes in the signals), in which we are interested.

III. Results and Discussion

We have studied how β is affected by the values of several technological parameters, taking as reference diode the one with the geometry and nominal values of the parameters shown in Fig. 1, based on real SBDs fabricated at the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN) [15]. In the simulations, the air is considered above the dielectric for the simulation domain represented in the figure (ϵ_{air}). The value of the ideal capacitance at zero bias, $C_{\text{Ideal}}(0)$, of the reference diode is equal to 307 pF/m. Initially, we have simulated diodes with different sizes of the Schottky contact L_{Sch} (results not shown), obtaining that, even if the total capacitance of the diode changes according to the linear scaling of the ideal capacitance with L_{Sch}, the EE parameter β remains the same, indicating that, as expected, EEs are mainly determined by the features of the diode at the right-hand side of the Schottky contact in Fig. 1.

To identify the physical origin of the capacitance, the local contribution to the total capacitance (per unit length) has been calculated as the variation of the charge (per unit length) between two bias points ($V_1 - V_b = -4.0$ V and $V_2 - V_b = -0.1$ V) divided by the voltage difference, as shown in Fig. 2 for several passivation dielectric materials, where red means a significant change in electron concentration with the applied voltage. The corresponding potential profiles are also shown in the figure. A noticeable influence of the passivation is evidenced both in the depleted area and the potential profile in the region at the right side of the Schottky contact, EEs being more pronounced for higher ϵ_{pas}. The values of the high-frequency EE capacitance ($C_{\text{EE}} = \beta_e \cdot \epsilon_{\text{sc}}$) corresponding to the cases shown in Fig. 2 are provided in Table I. As observed, C_{EE} is significant as compared to the ideal capacitance at zero bias $C_{\text{Ideal}(0)}$ even in the case of the lower dielectric constant (air).

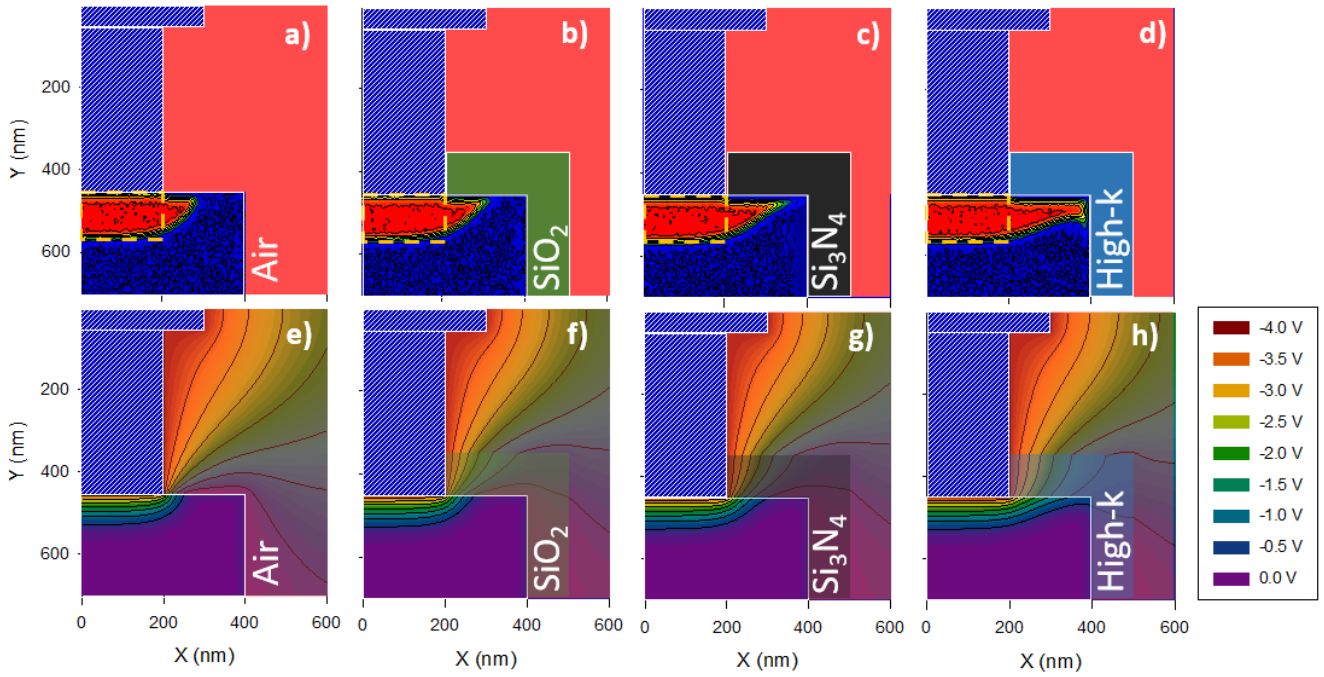

Fig. 2. (a)–(d) Maps of the local contribution to the total capacitance per unit length (where red means change in electron concentration with applied voltage) and (e)–(h) potential profiles (at $V - V_b = -4.0$ V) for different passivation dielectric materials: (a) and (e) air (absence of passivation), (b) and (f) silicon oxide, (c) and (g) silicon nitride, and (d) and (h) high-k dielectric. The geometrical parameters of the diode are those in Fig. 1. Only the region of interest, within the orange dashed rectangle of Fig. 1, is represented. The dashed rectangle in (a)–(d) delimits the ideal depletion region under the Schottky contact so that the EEs can be considered as mainly associated with the part of the depletion region outside this area.

TABLE I
VALUES OF THE HIGH-FREQUENCY EE CAPACITANCE AND RATIO WITH RESPECT TO THE IDEAL ONE CALCULATED AT ZERO BIAS IN THE REFERENCE DIODE OF FIG. 1 CONSIDERING DIFFERENT PASSIVATIONS

	Air	**SiO_2**	**Si_3N_4**	**High-k**
C_{EE}(pF/m)	48.2	65.1	87.4	123.0
$C_{EE}/C_{Ideal}(0)$	0.16	0.21	0.28	0.40

The maps of the electric potential of Fig. 2(e)–(h), corresponding to an applied voltage of $V - V_b = -4.0$ V, show how the potential changes with ϵ_{pas} both in the dielectric material and the lateral extension of the epilayer at the right of the Schottky contact. The change in the slope of the equipotential lines at the air–dielectric boundary is clearly observed in Fig. 2(f)–(h). A higher value of ϵ_{pas} allows a stronger penetration of the electric field in the lateral extension of the epilayer, thus leading an enlargement of the depletion at the origin of EEs, as observed in Fig. 2(a)–(d), and a higher associated β_e. The enhanced depletion also affects the occupancy of surface traps and, thus, β_T, as we will show in the following.

In the geometry of the diode, four are the parameters to be analyzed related to the presence of the dielectric passivation: type of dielectric material (dielectric constant, ϵ_{pas}), dielectric thickness (W_{diel}), the separation between the ohmic contact and the mesa (L_{sub}), and lateral extension of the epilayer (L_{EP}); the last two regions are covered by the dielectric. First, we have evaluated the influence of L_{sub}. Simulations for values of L_{sub} of 200 and 500 nm have been carried out (results not shown), which allows us to conclude that β is not affected by this parameter.

Next, we have focused on the dielectric thickness. In Fig. 3(a), β_e and β_T are represented as a function of W_{diel} (from 0 to 200 nm) for the four considered dielectrics. Of course, the case of air is independent of W_{diel} and coincides with the values corresponding to the other dielectrics when $W_{\text{diel}} = 0$ nm. As expected, EEs increase with W_{diel} and ϵ_{pas}, as observed in the figure. A thicker passivation layer, or an increase of its dielectric constant, helps to the penetration of the electric field into the semiconductor and, therefore, leads to an increase of the lateral depletion and the enhancement of the EE capacitance. The dependence of β_e and β_T on W_{diel} is similar, the values of β_T being systematically higher due to the additional contribution of the surface charges. This is due to the fact that the voltage variations do not completely reach the semiconductor since they are partially screened by the change of the surface charge so that the EE capacitance splits into two contributions: one coming from the free electrons and the other from the surface charges. In fact, in the case that no surface charge is considered in the simulations, the value of β_e is similar to that of β_T when using the SCCM.

The effect of the dielectric on the role played by the epilayer lateral extension L_{EP} in EEs is also relevant. Fig. 3(b) shows β_e and β_T as a function of L_{EP} for different dielectrics. As reported in a previous work for less realistic SBD geometries [20], β_e remains almost constant for long values of L_{EP}, but, for L_{EP} shorter than a given length, it significantly

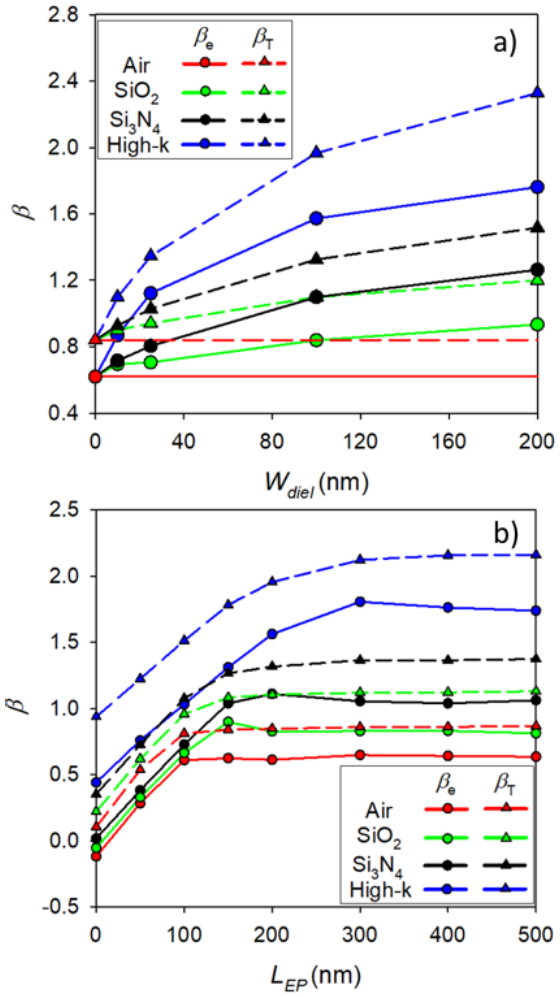

Fig. 3. β_e and β_T versus (a) W_{diel} with a distance between the ohmic contact and the mesa (L_{sub}) of 200 nm and (b) L_{EP} with $W_{\text{diel}} = 100$ nm for different dielectric materials.

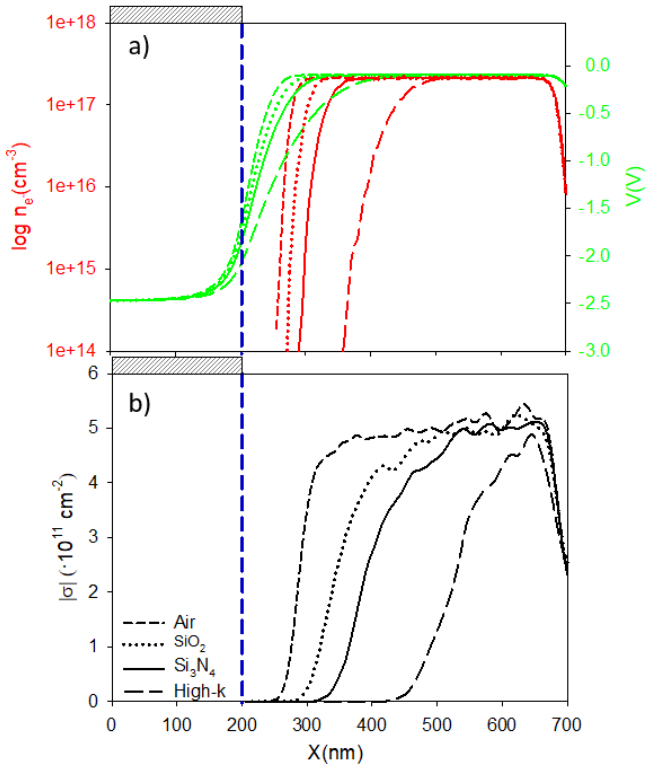

Fig. 4. Horizontal profiles of (a) potential and carrier concentration at 25 nm below the Schottky contact and (b) surface charge at the semiconductor/dielectric interface, represented from the Schottky contact to the corner of the epilayer, at $V - V_b = -4.0$ V, for air, SiO_2, Si_3N_4, and a high-k dielectric. $L_{\text{EP}} = 500$ nm. The blue dashed line indicates the limit of the Schottky contact.

decreases. β_T exhibits similar behavior. This behavior can be explained by the reduction of the lateral extension of the depletion region when the vertical sidewall of the epilayer (where surface charges are also present) starts to exert its influence. Interestingly, the value of L_{EP} at which β starts decreasing depends on the dielectric: the higher ϵ_{pas}, the higher the corner length (around 100 nm for air and 400 nm for the high-k dielectric). When the limit $L_{\text{EP}} = 0$ nm is reached, the EE capacitance is reduced to a certain value that again depends on the dielectric, β_e and β_T still being different because of the presence of surface charge at the vertical sidewall of the epilayer. For the dielectrics with lower ϵ_{pas}, small negative values of β_e are obtained, which means that EEs are completely suppressed and even inverted [20].

To illustrate, in more detail, the influence of the dielectric on the charges responsible for the EE capacitance, Fig. 4 shows the profiles of electron concentration and potential in the horizontal direction at a depth of 25 nm below the Schottky contact and the surface charge present at the semiconductor/dielectric interface from the Schottky contact to the corner of the epilayer. The electron concentration and potential are represented at a depth below the region depleted by the surface charge (if present). As already observed in Fig. 2, a higher ϵ_{pas} allows for deeper penetration of the electric field in the lateral extension of the epilayer, thus a longer region being depleted. Surface states, whose occupancy is self-consistently calculated with the carrier concentration in the proximity of the interface with the dielectric [19], are empty in the depleted region and then become occupied when moving away from the Schottky contact. For a long enough L_{EP}, like the case of the figure, the surface charge reaches similar values for the four dielectrics near the corner of the epilayer but differs when approaching the Schottky contact due to the different lateral depletion. Thus, the high-k dielectric exhibits a longer region where $\sigma = 0$ [see Fig. 4(b)] compared with the case of a dielectric with lower ϵ_{pas}. All these observations lead to more pronounced EEs, the higher ϵ_{pas} is both due to the depletion of the epilayer (characterized by β_e) and the release of electrons from the surface states (additional contribution included in β_T). In the case considered in the figure, the ratio between the high-frequency EE capacitance and the ideal capacitance at zero bias is 0.16 for air, 0.21 for SiO_2, 0.27 for Si_3N_4, and 0.45 for the high-k dielectric.

Despite that the use of a dielectric material of high ϵ_{pas} has the negative effect of increasing capacitive EEs, it may also be beneficial to improve the breakdown voltage of the SBD. As observed in the maps of the electric field shown in Fig. 5, corresponding to the most problematic region at the right side of the Schottky contact, as ϵ_{pas} is higher, along with a wider

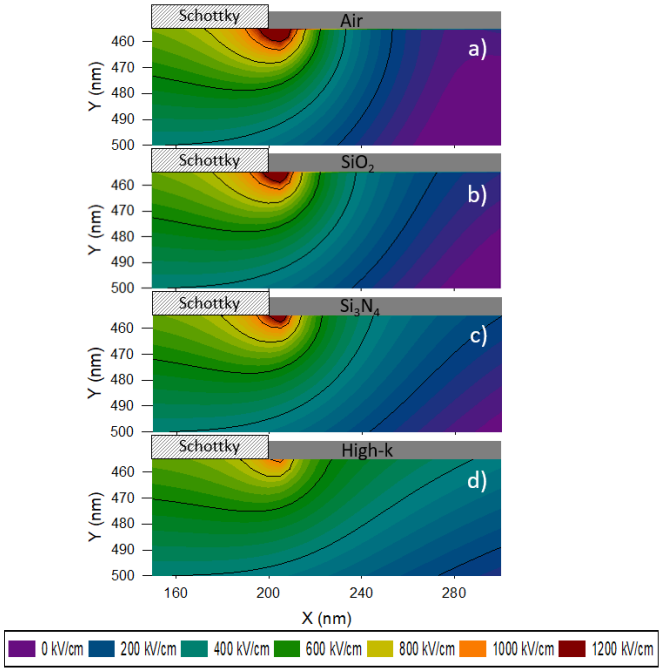

Fig. 5. Maps of the module of the electric field (in kV/cm) for the reference diode (see Fig. 1) and different passivation dielectric materials: (**a**) air, (**b**) SiO_2, (**c**) Si_3N_4, and (**d**) high-*k* dielectric. Only the semiconductor region around the border of the Schottky contact (corresponding to the blue dashed rectangle of Fig. 1) is represented.

extension of the high-field zone, the values are smoothed, and in particular, the maximum reached just at the edge of the contact is smaller. This fact is concomitant with the wider lateral extension of the depletion region, as already observed in Figs. 2 and 4.

The values of the capacitances provided so far correspond to a 2-D representation of (half of) a rectangular Schottky anode, assuming that the diode is homogenous in the nonsimulated dimension. Indeed, they are provided per unit length, normalized by the width of the diode. However, when reducing the size of the anode in order to increase the operation frequency, other geometries are used, such as the circular one shown in the inset of Fig. 1. In such a case, the absolute diode capacitance is given by $C_T(V) = C^T_{\text{ideal}} + C^T_{\text{EE}} = A\epsilon_{\text{sc}}/W(V) + L_{\text{contour}}\beta\epsilon_{\text{sc}}$ [10], where the absolute ideal capacitance C^T_{ideal} is proportional to the area of the anode A and the absolute EE contribution C^T_{EE} to the length of its contour L_{contour}. We neglect a second-order correction, independent of the geometry, associated with EEs accounting for the nonrectangular shape of the anode [3], [10]. In the case of a circular anode, $A = \pi r^2$ and $L_{\text{contour}} = 2\pi r$, with r being the radius of the anode, equivalent to L_{Sch} in our 2-D calculations considering that the simulation domain represented in Fig. 1 corresponds to half of a cut of the diode along its diameter. Fig. 6 represents the ideal capacitance at zero bias $C^T_{\text{ideal}}(0)$ and C^T_{EE} as a function of the radius of the anode in the reference diode of Fig. 1 considered to be circular. The values of the ratio $C^T_{\text{EE}}/C^T_{\text{ideal}}(0)$ (using β_e for the calculation of C^T_{EE} in order to account only for the high-frequency contribution to the EE capacitance) are also

TABLE II
VALUES OF THE RATIO BETWEEN THE HIGH-FREQUENCY EE CAPACITANCE AND THE IDEAL ONE CALCULATED AT ZERO BIAS FOR SEVERAL VALUES OF THE RADIUS OF THE ANODE AND DIFFERENT DIELECTRICS IN THE REFERENCE DIODE OF FIG. 1 CONSIDERED TO BE CIRCULAR

r (nm)	Air	SiO_2	Si_3N_4	High-k
100	0.63	0.85	1.14	1.60
200	0.31	0.42	0.57	0.80
400	0.16	0.21	0.28	0.40

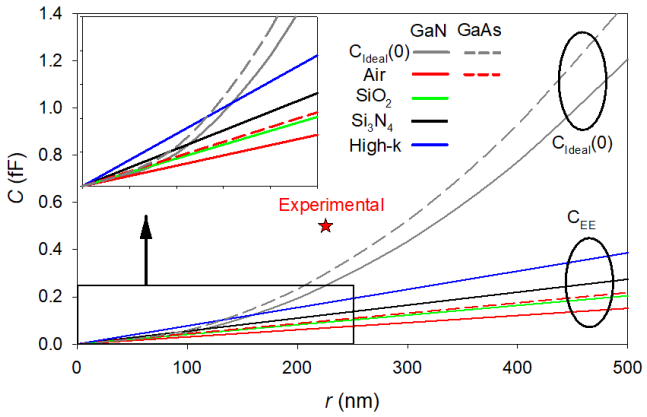

Fig. 6. $C^T_{\text{Ideal}}(0)$ and C^T_{EE} (for different dielectric materials) as a function of the radius r of the anode in the reference diode of Fig. 1 considered to be circular. The dashed lines correspond to GaAs, and the point is the experimental value for the total capacitance of the THz SBD of Maestrini *et al.* [23]. The inset shows a zoomed-in view of r from 0 to 250 nm.

provided in Table II. As observed, the EE contribution is quite significant compared to the ideal one, especially in small diodes passivated with high-permittivity materials, where C^T_{EE} may become the dominant contribution (the ratio $C^T_{\text{EE}}/C^T_{\text{ideal}}(0)$ increases linearly with r). For example, in the case of $r = 100$ nm, EEs produce a 63% increase in the diode capacitance, which would be further increased by the passivation with a 100-nm-thick Si_3N_4 layer to a 114%.

In order to compare the EE capacitances of GaN SBDs with the standard GaAs technology, the MC values obtained for the same diode but using GaAs as semiconductor are also shown in Fig. 6. The results of the simulations are in good agreement with the measurements of the capacitance of a small GaAs SBD of 0.16 μm^2 used for the fabrication of a 1.2-THz frequency mixer [23]. Please note that the ideal and EEs capacitances must be added up in order to be compared with the experimental result. Our simulations provide slightly lower values than the experimental 0.5 fF since no parasitic capacitance is considered in our case.

Fig. 6 also shows that, when comparing GaN and GaAs technologies, the lower dielectric constant of GaN helps to reduce the value of the total capacitance, thus allowing to use of larger anodes than for GaAs for the same target operation frequencies. On the other hand, the weight of the EEs in the total capacitance is the same in both technologies since both are proportional to the dielectric constant of the semiconductor.

IV. Conclusion

By means of 2-D MC simulations, we have analyzed the influence on EEs of the dielectric material used in the passivation of GaN planar SBDs. Due to EEs, the depletion region originated by the Schottky contact differs from the ideal one and penetrates into the lateral extension of the epilayer (L_{EP}), to a different extent depending on the passivation material. The results indicate that EEs can be minimized by the use of a material with a low dielectric constant (ϵ_{pas}), as well as reducing its thickness (W_{diel}). By reducing the value of L_{EP}, EEs decrease, the optimum value being the limit $L_{EP} = 0$ nm, for which the EE capacitance increases with the permittivity of the dielectric, as expected. In summary, the permittivity and thickness of the passivation dielectric material and the epilayer lateral extension are key points to reduce EEs, and careful attention must be paid when fabricating SBDs. The results obtained in this work allow us to optimize a real SBD geometry taking into account the restrictions that the technological process imposes on the fabrication of the devices.

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